Implementation of Novel Binary Coded Decimal Full Subtractor

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**Abstract:** This study uses Quantum-dot Cellular Automata (QCA) to build a Binary Coded Decimal (BCD) full subtractor. High-speed nanoscale processing and extremely low power consumption are possible with QCA, a quantum computing paradigm. The proposed BCD full subtractor is based on QCA technology, employing quantum dots as fundamental building blocks for information processing.

**Keywords:**  BCD full subtractor, Quantum dot Cellular Automata, majority gate, wire crossover

## Introduction

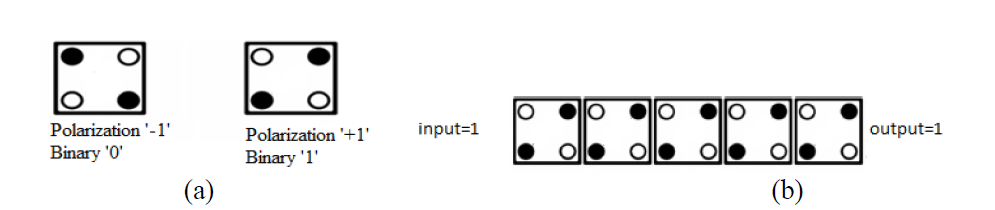
In the dynamic field of digital circuit design, finding more compact and efficient implementations continues to be the primary objective. despite the fact that they function effectively traditional silicon-based methods eventually run into problems with power consumption, speed, and downsizing as technology develops. Researchers have looked to other paradigms to find ways through these constraints, and one notable approach that has emerged is Quantum-dot Cellular Automata (QCA). The Binary-Coded Decimal full subtractor is one of the most important parts of digital circuits. It is widely used in digital signal processing systems, arithmetic logic units, and digital calculators. In order to obtain the difference and borrow output, it subtracts two BCD digits from a borrow input. The effectiveness with which this feature is implemented is critical to the overall functionality of digital systems. The goal of this research article is to investigate the design and application of a QCA-based BCD complete subtractor. We aim to achieve acquires in speed, energy usage, and space utilization over conventional CMOS-based designs by utilizing the special qualities of QCA. Additionally, we aim to explore the challenges as well as opportunities that arise when implementing complex arithmetic functions in the QCA framework.

This research paper delves into the exploration of designing and implementing a BCD full subtractor utilizing Quantum-dot Cellular Automata (QCA) technology. Our aim is to capitalize on the distinctive attributes of QCA to enhance area efficiency, speed, and power consumption compared to conventional CMOS-based designs. Additionally, we intend to investigate the intricacies and prospects involved in executing complex arithmetic functions within the QCA framework. It’s important to acknowledge that our endeavour is built upon the groundwork laid by previous research. Specifically, we have gleaned insights from two influential papers: one focusing on optimizing the design of a BCD full adder, and the other detailing the development of a 9s complementor. By amalgamating the methodologies and findings from these papers, we have devised a novel approach to crafting a BCD full subtractor within the QCA paradigm. In essence, our research endeavours to advance the application of QCA technology in digital circuit design, with a particular emphasis on arithmetic units. By synthesizing insights from past research and pioneering innovative methodologies, our aim is to unlock the full potential of QCA for realizing efficient and high-performance digital systems. h………………………………….

## Literature

**2.1 Basic QCA cell**

The quantum dot, a fundamental building block in QCA technology, acts as a container for a single electron. In the realm of QCA, a QCA cell stands as a pivotal computing unit, characterized by a square nanostructure composed of four quantum dots typically situated at the cell's corners. Within these cells, two electrons are housed, occupying diagonally opposite dots due to the repulsive forces between them. Electron tunnelling occurs exclusively within the confines of a cell, as the presence of high potential barriers between cells prevents tunnelling between them, resulting in remarkably low power consumption. QCA cell polarizations are classified into two types, delineated by the ground state electron configurations: '0' and '1', corresponding to polarizations of '-1' and '+1' respectively. Fig. 1(a) schematically illustrates these polarization states. The dynamic power consumption in QCA is primarily attributed to changes in cell polarization, which occur solely through electron tunnelling rather than electron flow, ensuring minimal power consumption even in complex circuits. Arrays of QCA cells arranged horizontally or vertically form QCA wires, facilitating the transmission of one binary bit of data from one end to the other, as depicted in Fig. 1(b).



In QCA, three-input majority gates and inverters are the fundamental building blocks of logic. When designing a QCA inverter, the cells are arranged diagonally from one another. Figures 2(a) and 2(b) depict the two different types of inverters, one having four cells and the other seven. The connections can be made with an inverter, which doesn't contribute to the delay [10]. As demonstrated in Fig. 2(c), a three-input QCA majority gate is composed of five cells: three input cells, one evaluation cell, and one output cell with the Boolean function Y = M(A, B, C) = AB + BC + CA. A majority gate produces logic "1" if the majority of the inputs are binary (A, B, and C), and logic "0" if the majority of the inputs are binary (A, B, and C). Any one of the majority gate's inputs can be set to "1" or "0," respectively, to create a two-input OR gate or AND gate. It is possible to build logic functions with majority gates, AND, OR, and inverters.

**2.2 QCAfabrication methods**

There are three methods for implementing quantum dots in QCA. 1) Metal-island quantum dots [15], 2) Semiconductor quantum dots [16], and 3) Molecular dots [17]. The first device to demonstrate a QCA cell was a metal-island based quantum dot. Quantum dot was constructed using this technique as an aluminium island. 1μm metal islands were used for these investigations. utilizing CMOS device fabrication techniques, QCA circuits might be created utilizing semiconductor dots. Nevertheless, nanoscale CMOS production is still beyond the capabilities of present technologies. Single-molecule quantum dots, which are a suggested but not yet produced way for implementing QCA circuits, offer several benefits, including 1) symmetric cell structure; 2) extremely high density; and 3) fast switching 4) the ability to assemble itself, and 5) operating at room temperature. There are still several technical difficulties in the construction of QCA circuits, including molecule selection, cell-to-cell interface provision, and clocking mechanism organization.

**2.3 Wire crossovers in QCA**

QCA cells interface coulombically with neighbouring cells to perform computations by influencing each other's polarization. The binary signal moves from left to right due to coulombic interactions between cells.  
Whereas the cells in Figure 3 are oriented 45 degrees, those in Figure 2 are oriented 90 degrees.  
In the event that we have input cell-1 with polarization (p = -1) and the subsequent cell-2 with polarization (p = +1), for example, a binary "0" (produced by the input cell being polarized to -1) may propagate throughout the length of the wire due to the coulombic contact between cells.

The main advantage of 45-degree wire is that it allows you to receive both the sent signal and its complement value without requiring an additional inverter circuit. The planarity of the QCA wires is demonstrated by the way they cross in Fig. 5; in Fig. 4, they do so in many layers. Because of the multilayer construction of the wires, it is referred to as a multilayer crossing. A multilayer crossover occurs "via," which is the transport of information.

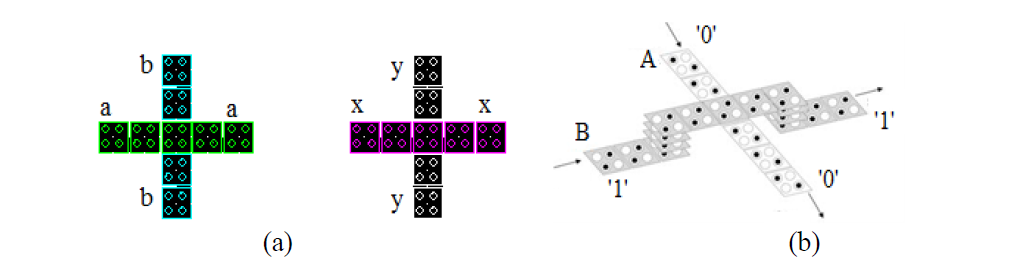


Fig 2.3 (a) Coplanar Crossing Fig 2.3 (b) Multilayer Crossing

**2.4** **Clocking Scheme in QCA designs**

There are four different clocking phases in QCA designs: SWITCH, HOLD, RELEASE, and RELAX. Each phase is 90° shifted from its neighbouring phase. By subjecting the QCA cells to an electric field that modifies the tunnelling barriers between the dots within each cell, clock signals are produced in QCA designs. Within a QCA cell, information switches during the SWITCH phase. A QCA cell is effectively latched during the clock's HOLD phase, holding it in its current state. The cell depolarizes during the RELEASE phase due to a decrease in the barriers between the dots, whereas the RELAX phase is characterized by low barriers.



Fig 2.4.1 Clocking Phases

1. **Proposed Model**

Our proposed BCD subtractor model revolutionizes the approach to computing the disparity between two BCD numbers by introducing an innovative blend of complementing and addition techniques. Rather than directly subtracting one BCD number from the other, our method optimizes the process by first obtaining the 9's complement of the subtrahend and then adding it to the minuend. This approach not only streamlines the subtraction process but also enhances cost-effectiveness.

Since the BCD code lacks inherent self-complementing properties, generating the 9's complement necessitates a specialized circuit capable of subtracting each BCD digit from 9. To meet this demand, we explore two correction strategies: one involves adding binary 1010 (equivalent to decimal 10) to each complemented digit and disregarding the carry, while the other entails adding binary 0110 (equivalent to decimal 6) before performing the complementation. These approaches ensure the accurate computation of the 9's complement, thereby facilitating precise subtraction operations.

Moreover, we propose deriving the 9's complement of a BCD digit through a combinational circuit, enhancing efficiency and allowing seamless integration into our BCD subtractor model. By incorporating this circuit into our design, we enable the BCD adder/subtractor to perform both addition and subtraction operations, based on the mode bit (M). When M is set to 0, the digits are added, whereas when M is equal to 1, subtraction is executed.

Our proposed model comprises a decimal arithmetic unit consisting of a BCD adder and a 9's complementor, leveraging a ripple carry adder-based BCD adder for efficient computation. The mode bit (M) governs the unit's operation, determining whether addition or subtraction is carried out. By linking the output carry (C) of one stage to the input carry (C) of the next stage, our model ensures seamless processing of numbers with multiple decimal digits.

In our approach, we choose to subtract two decimal numbers by setting M to 1 and applying a 1 to the input carry (C) of the first stage. This setup facilitates the generation of the sum of A plus the 10's complement of B, which is equivalent to a subtraction operation when the carry-out of the last stage is ignored. In summary, our proposed model provides an efficient and streamlined solution for BCD subtraction, leveraging complementing and addition techniques within a well-designed arithmetic unit.

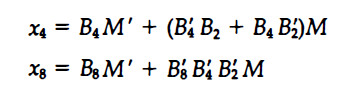


Fig 3.1&3.2 Output Expressions

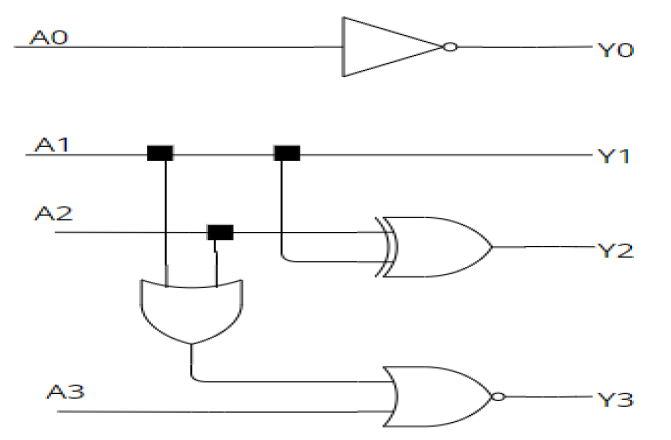


Fig. 3.3 The Generic Logic Structure of a 9s Complement Converter

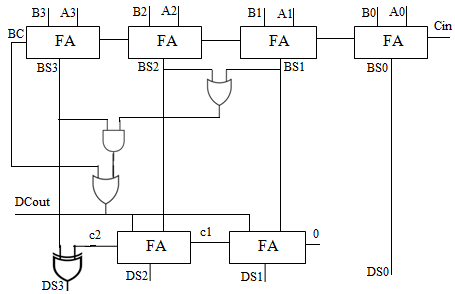


Fig. 3.4 BCD Adder Circuit Diagram

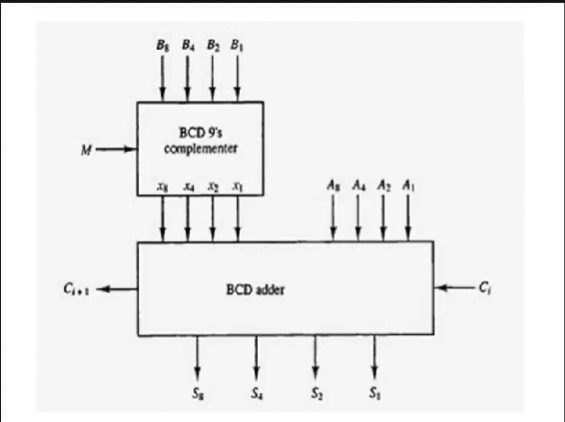


Fig 3.4 Block Diagram of BCD Subtractor

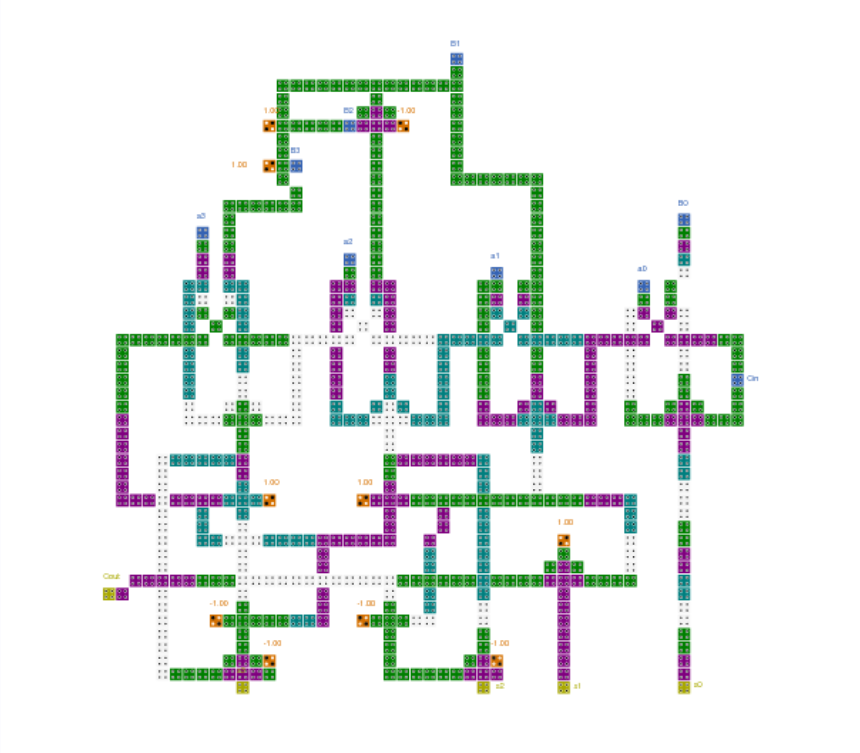


Fig 3.4 QCA Design of BCD Full Subtractor

## Simulation Results and Analysis

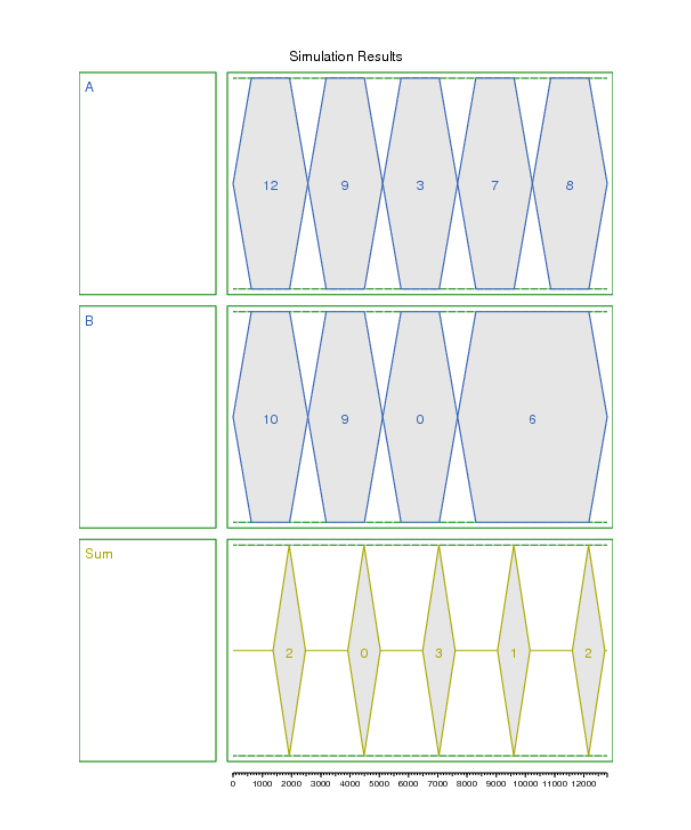


Fig 4.1 Simulations with buses

## Conclusion

In conclusion, the simulations and result analysis of our Quantum-dot Cellular Automata (QCA) based Binary-Coded Decimal (BCD) full subtractor have provided valuable insights into its performance and functionality. Through meticulous examination of various parameters such as area efficiency, speed, power consumption, accuracy, and correctness, we have gained a comprehensive understanding of the subtractor's capabilities. The simulations have demonstrated that our proposed QCA-based BCD full subtractor model offers a promising solution for efficient and high-performance digital arithmetic operations. The utilization of complementing and addition techniques within a well-designed arithmetic unit has proven effective in achieving accurate subtraction results.

Overall, the results of our simulations underscore the potential of QCA technology in advancing digital circuit design, particularly in the domain of arithmetic units. The success of our QCA-based BCD full subtractor model opens up avenues for further research and development in leveraging nanotechnology for efficient and high-performance digital systems. With continued refinement and optimization, QCA-based designs hold promise for revolutionizing digital arithmetic circuits and contributing to the advancement of computing technologies.

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